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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/632,024

07/31/2003

Gerard Chauvel

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EXAMINER

SWEARINGEN, JEFFREY R

ART UNIT

PAPER NUMBER

2445

NOTIFICATION DATE

DELIVERY MODE

12/15/2008

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No. 10/632,024	Applicant(s) CHAUVEL ET AL.	
	Examiner Jeffrey R. Swearingen	Art Unit 2445	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 September 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6,8-11,13-17 and 19-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6,8-11,13-17 and 19-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. In view of the appeal brief filed on 9/22/2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Nathan J. Flynn/

Supervisory Patent Examiner, Art Unit 2454.

Response to Arguments

2. Applicant's arguments with respect to claims 1-6, 8-11, 13-17, and 19-25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 8-11, 13-17, and 19-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Luo (US 6,169,700).

5. In regard to claim 1, Luo disclosed:

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a first processor that executes a transaction targeting a pre-determined address; column 4, lines 30-43

a second processor coupled to said first processor; and column 4, lines 30-43

a wait unit coupled to said first and second processors, said wait unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode, and said wait unit de-asserts the wait signal upon detection of a signal from said second processor. column 4, lines 30-43

6. In regard to claim 2, Luo disclosed:

the wait signal is de-asserted to permit the first processor to retrieve a status of the second processor. Luo detects when both processors are accessing the same memory address in column 4, lines 30-43. The addresses inputted to ADDR 1 or ADDR 2 are the instructions for the processor to execute, as in column 4, lines 1-7. The crossfeeding of the wait state signals and the ADDR information in column 6, lines 32-48 is where the wait state is released to detect if there is another wait state being asserted which would detect the status of the second processor based on the addresses being accessed.

7. In regard to claim 3, Luo disclosed:

said status includes one or more instructions that the first processor is to execute. Column 4, lines 1-7

8. In regard to claim 4, Luo disclosed:

said transaction comprises a read instruction. Column 4, lines 4-7

9. In regard to claim 5, Luo disclosed:

said transaction comprises a write instruction. Column 4, lines 4-7

10. In regard to claim 6, Luo disclosed:

said wait unit de-asserts the wait signal upon detection of a system interrupt signal generated by the first processor. RESET signal in column 5, lines 58-60

11. In regard to claim 8, Luo disclosed:

said wait unit upon detection of said signal asserts a processor interrupt signal to the first processor if the wait signal is already de-asserted. Column 6, lines 32-48

12. In regard to claim 9, Luo disclosed:

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executing a transaction that targets a pre-determined address; column 4, lines 30-43

detecting the transaction to said pre-determined address; column 4, lines 30-43

asserting a wait signal upon detection of the transaction to cause a processor to stall; column 4, lines 30-43

causing said wait signal to de-assert upon receiving a signal from another processor, said de-assert controlled by logic external to said processor. column 4, lines 30-43; RESET signal in column 5, lines 58-60

13. In regard to claim 10, Luo disclosed:

said stall comprises a low power mode. Column 5, lines 2-3 halts a processor. When a processor is halted, it is in a low power mode.

14. In regard to claim 11, Luo disclosed:

said event comprises a system interrupt. The RESET is the system interrupt. column 5, lines 58-60

15. In regard to claim 13, Luo disclosed:

said transaction is a read instruction to said pre-determined address. Column 4, lines 4-7

16. In regard to claim 14, Luo disclosed:

said transaction is a write instruction to said pre-determined address. Column 4, lines 4-7

17. In regard to claim 15, Luo disclosed:

a decode logic unit that determines when a first processor runs a transaction to a pre-determined address; column 4, lines 30-43

a first processor interface; column 4, lines 30-43

a second processor interface; and column 4, lines 30-43

logic coupled to the decode logic unit, the first processor interface, and the second processor interface, said logic asserts a signal propagated by the first processor interface to cause said first processor to stall; and column 4, lines 30-43

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said second processor interface receives a wait release signal from a second processor that causes the wait unit to de-assert the wait signal to said first processor through said processor interface.

column 4, lines 30-43

18. In regard to claim 16, Luo disclosed:

said transaction is a read instruction. Column 4, lines 4-7

19. In regard to claim 17, Luo disclosed:

said transaction is a write instruction. Column 4, lines 4-7

20. In regard to claim 19, Luo disclosed:

said wait release signal causes a processor interrupt signal to be asserted if the wait signal is already de-asserted. RESET signal, Column 6, lines 32-48

21. In regard to claim 20, Luo disclosed:

a system interrupt interface coupled to the logic, through which a system interrupt signal is received that causes the logic to de-assert said wait signal to said first processor through the first processor interface. RESET signal, column 5, lines 58-60

22. In regard to claim 21, Luo disclosed:

a first processor; column 4, lines 30-43

a second processor; column 4, lines 30-43

means for detecting a transaction targeting a pre-determined address and for asserting a wait signal to said first processor to cause the first processor to enter a wait state; and column 4, lines 30-43

means for releasing said first processor from the wait state by a wait release signal from said second processor. column 4, lines 30-43

23. In regard to claim 22, Luo disclosed:

the transaction comprises a memory read. Column 4, lines 4-7

24. In regard to claim 23, Luo disclosed:

the transaction comprises a memory write. Column 4, lines 4-7

25. In regard to claim 24, Luo disclosed:

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said means for releasing said first processor from the wait state comprises said second processor coupled to a wait unit, said wait unit de-asserts the wait signal upon detection of the wait release signal.

Column 4, lines 30-43

26. In regard to claim 25, Luo disclosed:

said means for releasing said first processor from the wait state comprises a system interrupt signal to a wait unit, said wait unit de-asserts the wait signal upon detection of the system interrupt signal.

RESET signal, column 5, lines 58-60

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

28. Baji US 5,740,404

29. Lannan et al. US 6,014,729

30. Jain US 6,954,873

31. Naji US 6,609,174

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. Swearingen whose telephone number is (571)272-3921. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Larry Donaghue can be reached on 571-272-3933. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Jeffrey R. Swearingen
Examiner
Art Unit 2445

/Jeffrey R. Swearingen/
Examiner, Art Unit 2445

/Larry D Donaghue/

Primary Examiner, Art Unit 2454

/Nathan J. Flynn/

Supervisory Patent Examiner, Art Unit 2454